Fluorinated Graphene in Interface Engineering of Ge-Based Nanoelectronics

Xiaohu Zheng, Miao Zhang, Xiaohua Shi, Gang Wang, Li Zheng, Yuehui Yu, Anping Huang, Paul K. Chu, Heng Gao, Wei Ren, Zengfeng Di,* and Xi Wang*

Germanium is a promising candidate to replace silicon in nanoelectronics due to its significantly higher electron and hole mobilities. However, the unstable germanium oxide formed at the interface between the channel and dielectric layer has impeded the progress of Ge-based nanoelectronics. By taking advantage of the impermeability of graphene, it is discovered that the insulating fluorinated graphene is able to act as an efficient diffusion barrier layer to suppress the formation of the unstable interfacial oxide in Ge-based devices. The Ge-based device with the fluorinated graphene exhibits negligible capacitance versus voltage hysteresis, extremely low leakage, and superior equivalent oxide thickness. First-principles calculations reveal that interfacial diffusion, which would otherwise be unmanageable, is sufficiently obstructed by the fluorinated graphene. This new structure is expected to expedite the implementation of germanium as a channel material in next-generation nanoelectronic devices.

1. Introduction

Aggressive scaling of silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices is approaching the fundamental physical limit of Si and further progress requires alternative channel materials with high carrier mobility. Germanium (Ge) possesses not only higher electron mobility but also the highest hole mobility of all known semiconductor materials and is a promising candidate to replace Si in future low-power logic applications.[1–3] In addition, on the heels of the perfect integration of silicon dioxide (SiO_2) into silicon-based devices, Ge seems more compatible with the established CMOS technology than other potential channel materials.[4,5] In fact, Ge is not new to the integrated circuit (IC) industry. The first transistor and first IC invented in 1947 and 1958, respectively, were produced using Ge instead of Si. However, the unstable germanium oxide has forced the IC industry to adopt Si as the mainstream substrate and this fundamental obstacle has remained for almost 60 years.[4] GeO_2, which is readily formed at the interface between the dielectric layer and Ge substrate, is rather unstable and can be thermally decomposed into several GeO_x suboxides,[6] resulting in a high density of dangling bonds at the interface.[7] These interface defect states, which cannot be passivated by conventional annealing,[1,7,8] degrade the intrinsically high carrier mobility and increase the off-state leakage current and subthreshold turn-off.[9] Furthermore, since wet processes are adopted in IC processing, the water-soluble Ge oxide creates another hurdle and solutions such as the use of high-*k* dielectrics, effective surface passivation, insertion of a Si capping layer, and so on have been proposed.[10–16] However, the formation of Ge–O bonds at the interface between the Ge and dielectric film is still unavoidable. Even though the incorporation of metal or nitrogen (N) into the interfacial GeO_2 layer, e.g., GeON,[17] GeAlON,[18] GeOS,[19] YscGeO,[20] has been found to stabilize the high-*k*/Ge interface and improve the electrical characteristics of Ge-based devices, the uncontrollable and non-stoichiometric nature of the interfacial oxide do not bode well for IC processing which requires tight control. Furthermore, since the dielectric constant of the interfacial oxide, regardless of whether it is stable or unstable, is much lower than that of the high-*k* dielectrics, the equivalent oxide thickness (EOT) of the gate dielectrics cannot reach the predesigned value. Consequently, total absence of Ge oxide is preferred at the high-*k*/Ge interface but it is fundamentally difficult.

Graphene is the thinnest known material and also the strongest. It has been demonstrated that the monolayer

Dr. X. Zheng, Prof. M. Zhang, X. Shi, Dr. G. Wang, Dr. L. Zheng, Prof. Y. Yu, Prof. Z. Di, Prof. X. Wang
State Key Laboratory of Functional Materials for Informatics, Shanghai Institute of Microsystem and Information Technology
Chinese Academy of Sciences
865 Changning Road, Shanghai 200050, China
E-mail: zfdi@mail.sim.ac.cn

Dr. G. Wang
School of Physical Science and Technology, Lanzhou University
Lanzhou 730000, China

Prof. A. Huang
Department of Physics, Beihang University
Beijing 100191, China

Prof. P. K. Chu
Department of Physics and Materials Science
City University of Hong Kong, Tat Chee Avenue
Kowloon, Hong Kong, China

H. Gao, Prof. W. Ren
International Centre for Quantum and Molecular Structures and Department of Physics, Shanghai University
Shanghai 200444, China
E-mail: renwei@shu.edu.cn

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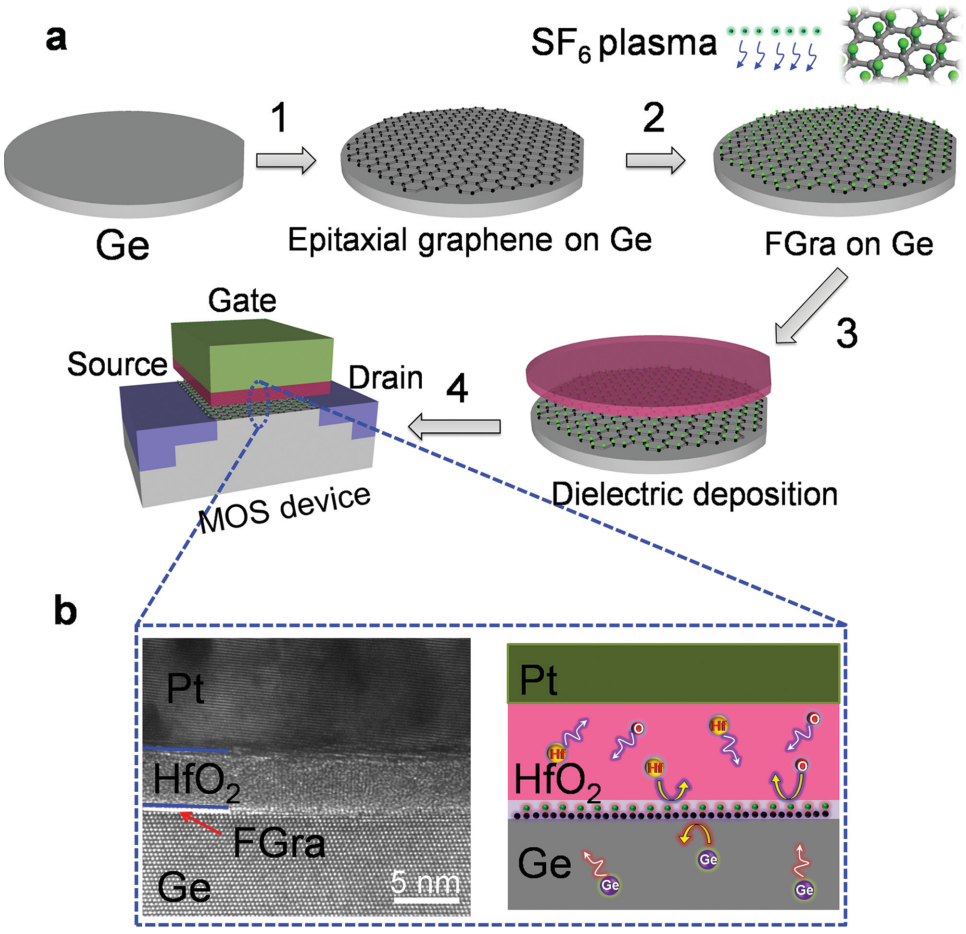

Figure 1. a) Schematic diagram showing the implementation of FGra as the diffusion barrier layer between the Ge substrate and HfO_2 dielectric layer in the Ge-based MOS device: (step 1) direct growth of continuous monolayer graphene on Ge; (step 2) FGra synthesized by exposure to SF_6 plasma; (step 3) dielectric deposition on FGra/Ge by atomic layer deposition; (step 4) MOS device completed by standard semiconductor manufacturing processes. b) Cross-sectional high-resolution TEM of the gate stack showing the absence of interfacial oxide formation in the presence of FGra and schematic diagram showing retarded diffusion in the vicinity of high-*k*/Ge interface.

graphene is impermeable to gases[21] and can act as an effective barrier to protect Cu, Fe, and Cu/Ni from oxidation.[22–24] Hence, graphene may also be an effective barrier to impede interdiffusion between the Ge and gate dielectrics, and to suppress the formation of unstable interfacial oxide. As intrinsic graphene has a zero bandgap and may deteriorate the capacitive performance of MOS devices (Figure S1, Supporting Information), fluorinated graphene (FGra) can be employed as a wide bandgap and high-quality 2D insulator.[25–32] In this work, taking advantage of recent breakthrough in direct epitaxy of a single-crystal graphene monolayer on Ge,[33,34] we integrate FGra into Ge-based CMOS devices as the diffusion barrier layer between Ge and gate dielectrics. By means of fluorination, the epitaxial graphene derivative, that is, FGra, is incorporated into the Ge-based device between the channel and gate dielectrics, as schematically illustrated in **Figure 1**. The FGra acts as an efficient diffusion barrier to suppress the formation of unstable Ge oxide and the high-performance Pt/HfO_2/FGra/Ge MOS capacitor with negligible capacitance versus voltage (*C*–*V*) hysteresis, extremely low leakage, and superior EOT is obtained.

2. Results and Discussion

Raman scattering is performed to monitor the fluorination process of the graphene/Ge system (see Figure S2, Supporting Information). Fluorination induces the formation of sp^3 hybridization of carbon (C) atoms and C-F bonds as well as restructuring of the intrinsic sp^2 characteristic of graphene. This is verified by comparison with the C1s core-level spectra obtained by X-ray photoelectron spectroscopy (XPS) from the pristine graphene and FGra as shown in **Figure 2**a. In the pristine graphene, the major peak at 284.6 eV originates from nonfunctionalized sp^2 C atoms[35] whereas the minor peaks at 285.1 and 286.7 eV are attributed to aliphatic sp^3 C atoms produced by hydrogen (H) and oxygen (O) contamination, respectively[36] (see Figure S3, Supporting Information). In the FGra, the enhancement of the peak at 285.1 eV (sp^3) together with the attenuation of the peak at 284.6 eV (sp^2) is believed to be associated with distorted sp^2 C atoms with one neighboring C atom bonded to one fluorine (F) atom (C–CF).[37] The pronounced F1s peak at 688.5 eV (inset in Figure 2a) and extra component at 289.5 eV in the C1s peak suggest the existence

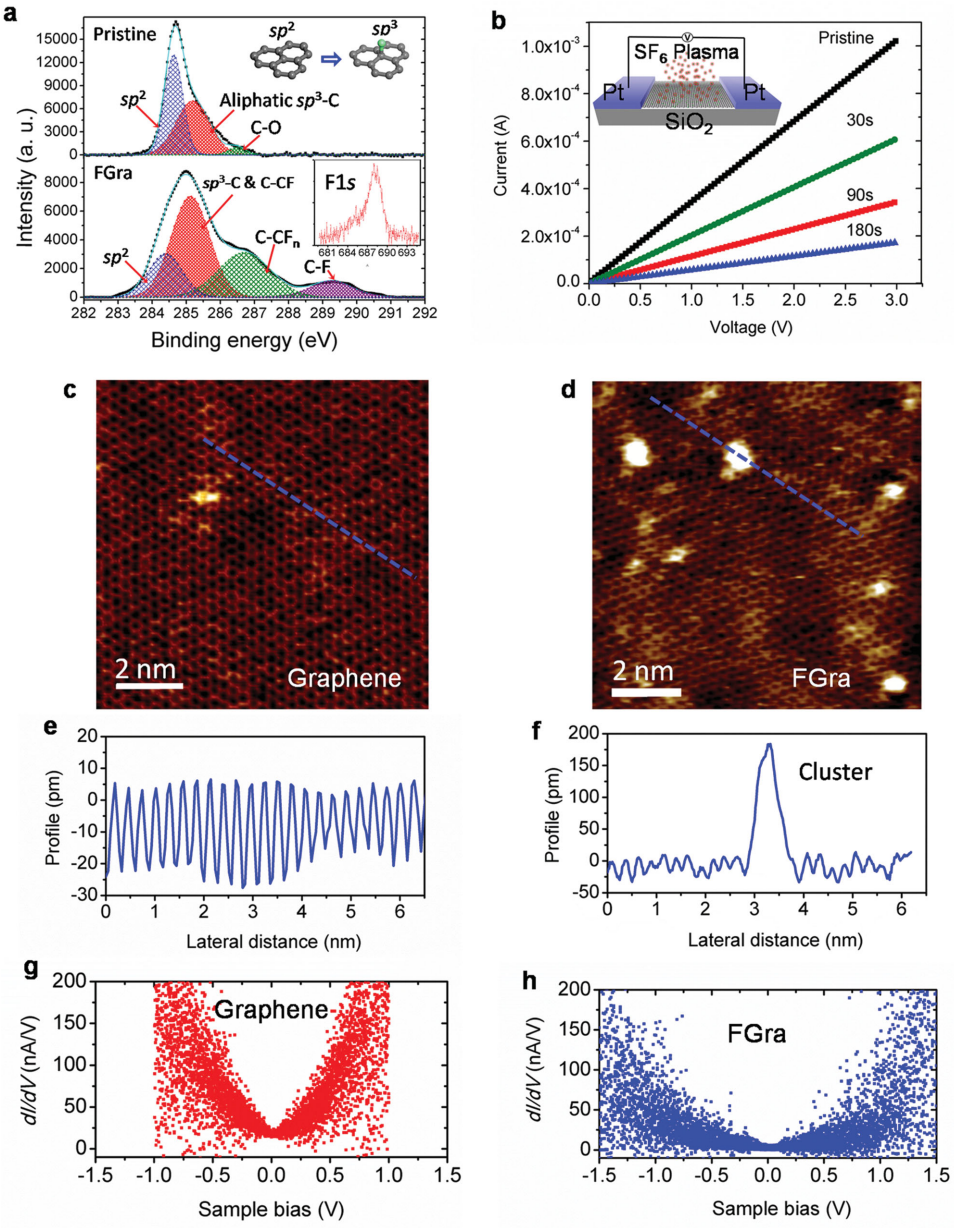

Figure 2. a) Comparison of the XPS C1s spectra between the pristine graphene and FGra. The upper inset presents the transition from the planar sp^2 to tetrahedral sp^3 configurations and the F1s peak of the FGra is shown in the lower inset. b) *I–V* characteristics of the FGra showing that the conductivity decreases and surface resistance increases as the fluorination time is increased. c,d) STM images of the pristine graphene and FGra, respectively. e,f) Line scans acquired from (c,d), respectively. g,h) Differential conductance spectra acquired from the graphene in (c) (red dots) and FGra in (d) (blue dots).

of F atoms and F–C bonding.[38] The effect of fluorination on the surface resistivity of graphene is investigated after transferring to an oxidized Si wafer, as shown in Figure 2b. Graphene transfer process and the fabrication of two-terminal device are presented in Section IV, Supporting Information. As the fluorination proceeds, the current value decreases dramatically, indicating the rapid reduction of conductivity of the fluorinated graphene obtained, as observed by others.[27,32,39] The scanning tunneling microscopy (STM) image in Figure 2c acquired from graphene on highly doped p-Ge discloses the honeycomb structure of pristine graphene at a sample bias of 100 mV. The line scan acquired from the topographic image is presented in Figure 2e and the blue line in Figure 2c delineates the position. The data show a 2.5 ± 0.1 Å modulation feature, which agrees with the theoretical value of graphene lattice constant (2.46 Å). However, the STM topography of FGra obtained at the same sample bias changes significantly, as shown in Figure 2d. The corresponding line scan in Figure 2f indicates membrane deformation and clustering due to absorption of F atoms. The local states in both samples are investigated by selection scanning tunneling spectrum (STS) at the same areas where the STM images are acquired. The pristine graphene (red dots in

Figure 2g) exhibits the typical semimetallic differential conductance[40] and displays a minimum (the Dirac point) at near zero sample bias. The FGra layer (blue dots in Figure 2h) shows virtually no differential conductance over an energy range of approximately ±0.75 V, indicating a wide bandgap in the FGra.[40] Based upon the various FGra structures, our first-principles calculations (see Figure S4, Supporting Information) also demonstrate the existence of bandgap (1.63 eV for C_2F armchair configuration and 1.52 eV for C_2F boat configuration) in the FGra with single-sided fluorination. Previous and our present calculations suggest that a stable C_4F structure (with lower F concentration) could even have a bandgap as large as ≈3 eV.[39] When further reducing F content to a C:F ratio of 8:1, we obtain calculation results (not shown) that bandgaps vary from ≈0.8 to 0 eV if considering a number of different structures of $C_{32}F_4$. We therefore propose that all the aforementioned gap model structures coexist in the FGra as consistent with the STS measurements.

The impermeability of FGra is studied by comparing the oxidation behavior of bare Ge and FGra-coated Ge (see Figure S5, Supporting Information). It is found that the FGra exhibits superior impermeability to provide adequate protection against the external oxidation of Ge underneath. To further investigate how FGra acts as an efficient diffusion barrier layer between the high-*k* dielectric layer and Ge substrate, a 20 nm thick HfO_2 layer is deposited on both the bare Ge and FGra/Ge substrate followed by conventional post-deposition annealing[41] at 500 °C in N_2 for 1 min to achieve a stable interface. Cross-sectional high-resolution transmission electron microscopy (HR-TEM) and XPS are performed to compare the interfacial layers (ILs). As shown in **Figure 3**a, an amorphous phase with a variable thickness of 1–1.5 nm appears from the rough interface between the HfO_2 dielectric layer and bare Ge substrate. In contrast, in the presence of the FGra barrier layer, formation of the amorphous IL is suppressed completely. Owing to the monolayer feature of the FGra, the IL between the HfO_2 dielectric layer and Ge substrate is extremely thin and flat as shown in Figure 3b. The chemical bonding states in the IL are determined by XPS depth profiling. Figure 3c,d show the evolution of the $Ge2p_{3/2}$ core level peak at different sputtering time. As shown in Figure 3c, the peak at 1220.3 eV corresponding to the +4 oxidation state of Ge[42] is detected from the HfO_2 dielectric layer initially suggesting the generation of GeO_2 by interdiffusion between Ge and the dielectric layer.[43] With increasing sputtering time, the peak shifts gradually from the +4 oxidation state to the Ge suboxides states and finally the Ge substrate (0 state). The transformation of GeO_2 (+4 state) to Ge (0 state) indicates the presence of the IL layer in which the suboxide species (GeO_x) are contained. In contrast, after addition of the FGra barrier layer, Ge is barely detected from the HfO_2 dielectric layer. The sole peak corresponding to elemental Ge emerges at the interface between the HfO_2 dielectric layer and Ge substrate while there are no peaks stemming from suboxide species (GeO_x) or dioxide species (GeO_2), indicating

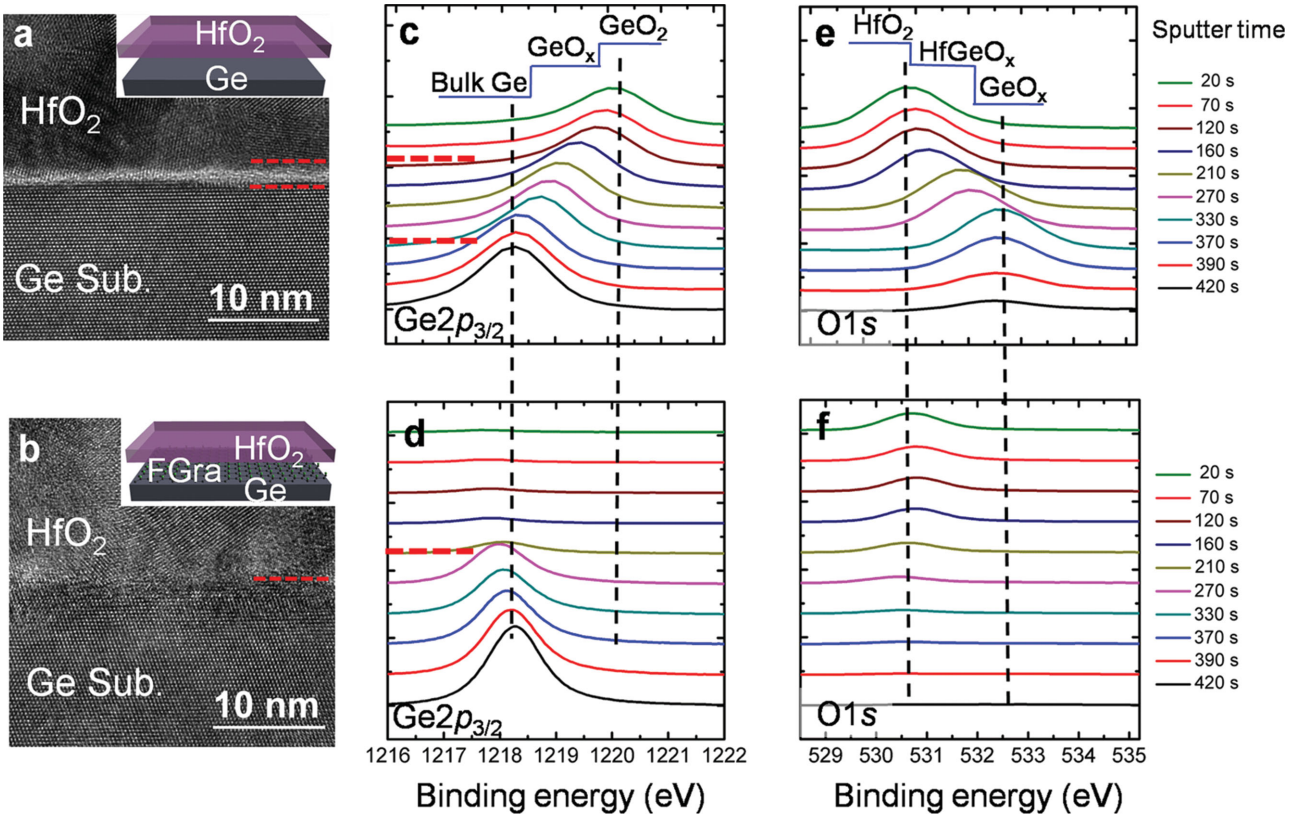

Figure 3. HR-TEM images acquired from the IL from both a) Ge/HfO_2 and b) Ge/FGra/HfO_2 stacks. c,d) XPS depth profiles of the $Ge2p_{3/2}$ core level peak acquired from (a,b), respectively. e,f) XPS depth profiles of the O1s core level peak acquired from (a,b), respectively. The absence of Ge related oxides in (d,f) suggests that the FGra acts as the efficient diffusion barrier layer between the high-*k* dielectric layer and Ge substrate.

that the formation of Ge oxides is completely suppressed in the presence of the FGra diffusion barrier (Figure 3d). The similar phenomenon is observed from the O1s spectra in Figure 3e,f. Without the FGra layer, the O signal shifts from the Hf oxide state to Ge suboxides states but after addition of the FGra layer, only the peak corresponding to HfO_2 is observed while Ge related oxide is barely seen. The results provide strong evidence that the FGra with superior impermeability impedes interdiffusion between the high-*k* dielectric layer and Ge substrate and suppresses IL formation.

To elucidate the physical mechanism governing the observed diffusion barrier effects of FGra, an improved version of the nudged elastic band (NEB) method proposed by Henkelman and Jónsson[44] is adopted to calculate the barrier height of one O or Ge atom penetrating the graphene and FGra. The energy of the adsorbed O or Ge atom on different sites of the graphene is calculated as shown in **Figure 4**a,e, respectively. The three positions on the honeycomb lattice, namely, bridge (B), hollow (H), and top (T) are considered, and our results reveal that both the O and Ge atoms adsorbed on the graphene are most stable on the bridge site, followed by the top and hollow sites with higher energies. Figure 4b shows the energy barriers during the course of O penetration following the fixed vertical path via the hole at the center of the graphene hexagon. An enormous barrier energy of about 16 eV needs to be overcome if O atoms diffuse by this route and hence, the hole at the center of the graphene hexagon is not the energy-efficient diffusion route. The alternative diffusion route shown in Figure 4c starts from the most stable configuration of an O atom adsorbed on the pristine graphene, i.e., the bridge geometry. It is found that the adsorbed O atom preserves the bridge configuration with two neighboring C atoms, and the penetration process is accomplished by gradually flattening the C–O–C bridge bond and switching the position from one side to the other side of the graphene, as depicted by the snapshots corresponding to the various stages in Figure 4c. The minimum energy barrier is still as large as about 6 eV, which is big enough to block possible diffusion. The calculated values of the energy barriers are quantitatively consistent with the previous study.[45] When one side of the graphene is fluorinated to form FGra, a similar energy barrier height for the penetration of O atoms by the bridge diffusion route is obtained, indicating that the FGra also possesses superior impermeability to O atoms (Figure 4d).

The possible diffusion behavior of Ge atoms from the bottom side to the top side in pristine graphene or FGra is also investigated by the improved NEB method. As the radius of the Ge atom is larger than that of the O atom, the passage of the Ge atom from the bottom to the top through the hole at the center of the hexagon is impossible. Therefore, only Ge adatoms on the graphene in the bridge geometry and the top geometry are considered as the initial configurations. On account of the different chemical reactivity between Ge and O with graphene, the penetration of Ge atoms through the gradually flattening the C–Ge–C bridge bond needs to overcome a considerable energy barrier of 14 eV (Figure 4f), which is even larger than that of the O atom with the same geometry. Figure 4g shows the energy barriers in the Ge penetration process starting from the top configuration. According to the snapshots of the atomic structures at various stages, the Ge atom substitutes its nearest C atom, pushes the C atom out to the bridge position (inset in Figure 4g), recalls the C atoms, and makes penetration. Figure 4g suggests an overall energy barrier as large as 9 eV, indicating the excellent impermeability of pristine graphene to Ge atoms. As F atoms are attached to the top side of graphene in the FGra, Ge diffusion starting from the top configuration becomes rather complicated and the reaction between Ge and F is prone to occur after the passage of Ge atoms. Complete passage of Ge atoms through the FGra still needs to overcome an energy barrier of more than 7 eV, as shown in Figure 4h and consequently, owing to the huge energy barrier for O or Ge atom penetration, both graphene and FGra exhibit superior impermeability and hence to hinder diffusion of O or Ge atoms from either side.

MOS capacitors with HfO_2 gate dielectrics of various thicknesses are fabricated. The high-frequency (1 MHz) *C*–*V* characteristics of the Pt/HfO_2/Ge capacitors without FGra and with FGra as a function of different sweeping voltages are depicted in **Figure 5**a,b, respectively. The capacitance is measured by sweeping the voltage from inversion to accumulation and the thickness of the dielectric layer is determined by TEM (Figure S6, Supporting Information). With regard to the HfO_2/Ge gate stack without FGra, the hysteresis of the flatband voltage (ΔV_{FB}) is found to be 300 mV when the gate voltage is swept in the range of ±1 V, as shown in Figure 5a. The hysteresis increases gradually as the sweeping voltage increases and becomes as large as 1.45 V when the sweeping range is extended to ±2.5 V. On the other hand, when FGra is integrated into HfO_2/Ge gate stack, negligible hysteresis is observed even in the sweeping range of ±2.5 V as shown in Figure 5b. The hysteresis arises from the interfacial defects at the inferior dielectric/semiconductor interface. The large *C*–*V* hysteresis observed from the HfO_2/Ge gate stack is believed to be due to defects in the formed IL easily created by partial intermixing of Ge and HfO_2.[46] The defects in the nonstoichiometric IL generally have diverse trap levels.[47] Therefore, as the sweeping range is extended, more defects in the IL are involved in the charge-state transition process resulting in larger *C*–*V* hysteresis (Figure 5a). As shown in Figure 5c, the forward and reverse *C*–*V* curves obtained from the Pt/HfO_2/FGra/p-Ge with different HfO_2 thicknesses show excellent *C*–*V* characteristic with negligible hysteresis, indicating that the interfacial defects scarcely exist in the presence of FGra. According to the high-frequency (1 MHz) accumulation capacitance shown in Figure 5a, the dielectric constant, *k*, of the gate dielectrics of the HfO_2/Ge gate stack is estimated to be 8, which is significantly smaller than that of bulk HfO_2 (18–20) with the amorphous or monoclinic structure[48] due to the presence of the IL. However, as shown in Figure 5c, when the FGra is incorporated into the HfO_2/Ge gate stacks, the *k* values of the gate dielectrics are in the range of 15–18 when the dielectrics thicknesses vary from 13.5 to 4.5 nm, which is comparable with pure HfO_2.[48] Preservation of the dielectric constant further confirms that the FGra acts as an effective Ge diffusion barrier and suppresses IL formation. In particular, when a 4.5 nm HfO_2 is used, the EOT can be reduced to 1 nm which can even satisfy the requirement as the downscaling of Si-based CMOS devices is approaching 10 nm technology node and beyond.[2,49] Figure 5d shows the leakage current density of the Pt/HfO_2/Ge capacitors without

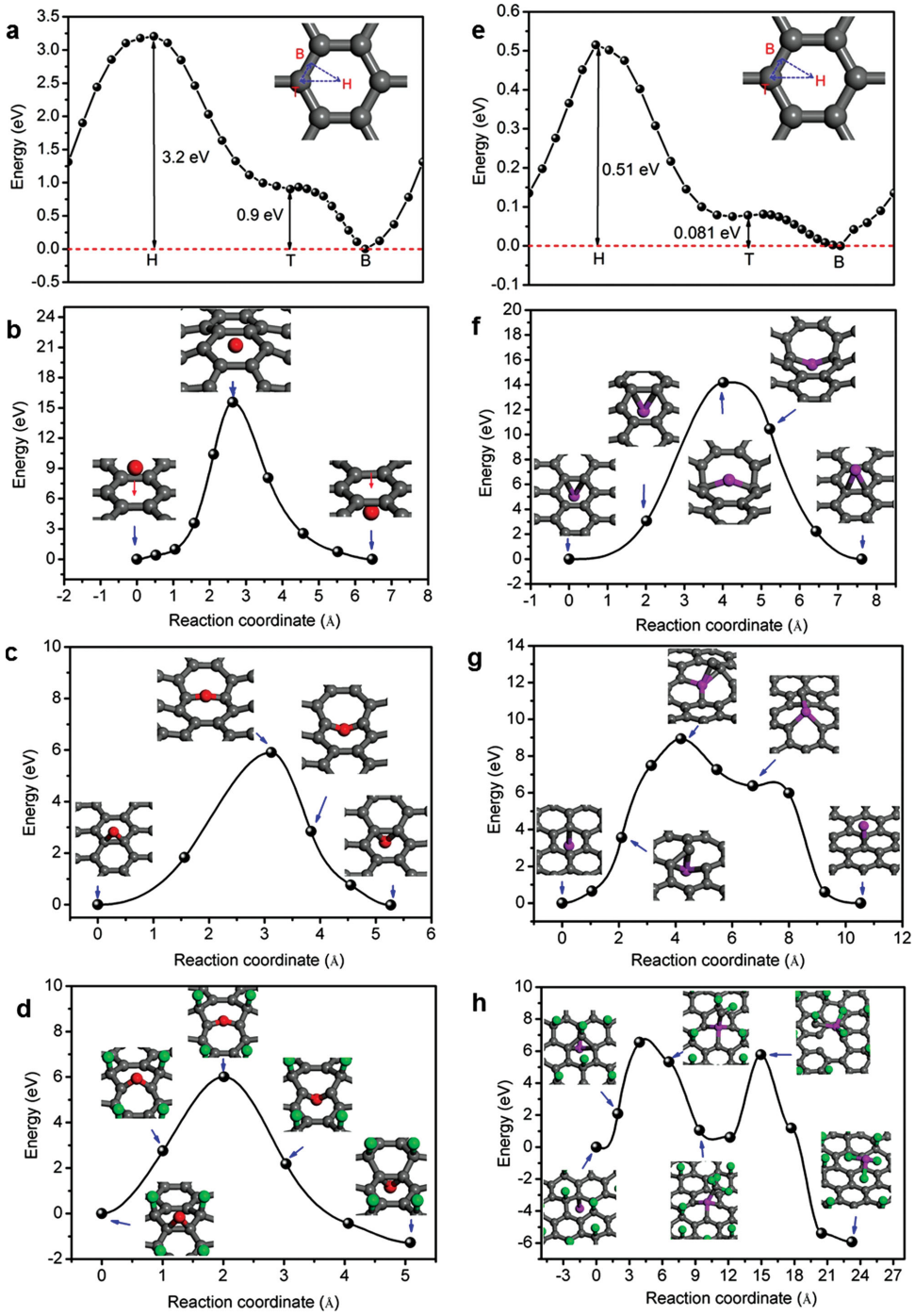

Figure 4. a,e) Energy variations of adsorbed O and Ge atoms along the H (hollow),T (top), and B (bridge) sites of a hexagon of graphene showing that both the O and Ge atoms are most stable on the bridge site, followed by the top and hollow sites with higher energies. b) O atom penetrating through the center of the graphene hexagon (hollow to hollow). c) O atom penetration with the bridge patch through the formation of C–O–C bridge bond. d) Energy barrier height of O penetration through the FGra formed by the attachment of F atoms on one side of graphene. f) Ge atom penetration with the bridge patch through the formation of C–Ge–C bridge bond. g) Penetration of Ge atom through graphene starting from the top geometry. h) Penetration of Ge starting from the top geometry of FGra.

FGra and with FGra. A leakage current density as high as 1 A cm^{-2} is observed from the Pt/HfO_2/Ge capacitor without FGra but the FGra-incorporated one shows a leakage current density suppressed by more than four orders of magnitude. As the gate voltage is changed between –3 and +3 V, the leakage current density is observed to be as small as 3×10^{-4} A cm^{-2}, which obviously demonstrates the excellent performance of the Pt/HfO_2/Ge gate stack with the FGra.

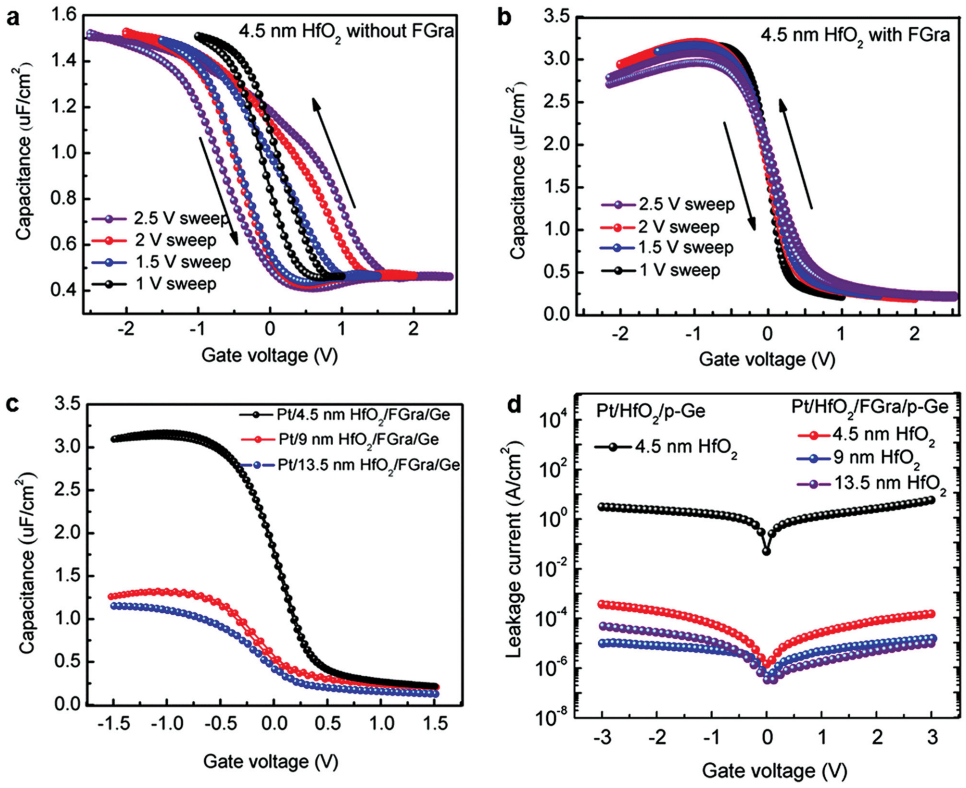

Figure 5. High-frequency (1 MHz) *C–V* characteristics of the Pt/HfO_2/Ge MOS capacitors as a function of sweeping voltages: a) without FGra and b) with FGra. c) Forward and reverse *C–V* curves acquired from the Pt/HfO_2/FGra/p-Ge with different HfO_2 thicknesses. d) Comparison of the gate leakage currents between the Pt/HfO_2/Ge MOS capacitors with and without the FGra.

3. Conclusion

Continuous downscaling of Si-based CMOS devices demands alternative technology such as the combination of high-*k* dielectrics with Ge to overcome serious problems related to the large leakage current and significant mobility degradation. However, owing to the inevitable formation of unstable Ge oxides, the inferior interface quality impedes the adoption of high-*k*/Ge gate stacks. In this work, FGra is incorporated into a Ge-based MOS device as the diffusion barrier layer. The FGra is able to totally suppress the formation of unstable Ge related oxides to yield a perfect interface with negligible IL defects. The MOS capacitor with the Pt/HfO_2/FGra/Ge structure exhibits high performance with negligible hysteresis and extremely low leakage. The novel interface engineering technique is expected to expedite the development and acceptance of Ge-based nanoelectronic devices.

4. Experimental Section

Ge-Based MOS Stacks Fabrication: Highly doped p-type Ge (175 μm thick, AXT) substrates with resistivity of 0.01–0.05 Ω cm were cleaned by dipping them in diluted 7% HCl for 10 s, 5% HF for 15 s, and deionized water for 20 s. This procedure was repeated five times to remove the native oxide completely. Fabrication of graphene was carried out in a horizontal tube furnace as described previously.[33] Fluorination of graphene was performed by exposing the sample in the SF_6 plasma in the OXFORD Plasma Lab system-100. To avoid potential etching of graphene, the sample was placed back to the SF_6 plasma. The SF_6 flow rate was as low as 40 sccm and plasma power was 50 W. During fluorination, the chamber pressure and temperature of the sample stage were 96 mTorr and 60 °C, respectively. The dielectric layer (HfO_2) was grown on an atomic layer deposition (ALD) system of BENEQ TFS-200 at about 200 °C. Liquid tetrakis (ethylmethylamino) hafnium (TEMAH) of 99%+ purity was the hafnium precursor and H_2O was the oxidant. About 100 nm of platinum (Pt) was sputtered as the electrode by magnetron sputtering onto the HfO_2 with a shadow mask. Finally, the capacitors were rapid thermal annealed (RTA) at 400 °C in N_2 for 1 min.

Characterization: Raman scattering (HORIBA Jobin Yvon HR800) was conducted using an Ar^+ laser with a wavelength of 514 nm and a spot size of 1 μm. The spectra were recorded with a 600 lines mm^{-1} grating. The Bruker Multimode 8 system was utilized to perform the AFM, STM, and STS measurements. The STM images were acquired using the constant-current mode by providing a current setpoint of 1.2 nA under the sample bias of 100 mV in the normal ambient. The ESCALAB 250 XPS manufactured by Thermo VG Scientific Ltd. was employed to study the chemical states of the surface and interface with monochromatic the Al K_α X-ray source. All the measurements were performed in an ultra-high-vacuum chamber at a base pressure of 10^{-10} Torr at room temperature. Depth profiling at a sputtering rate of about 0.15 nm s^{-1} was performed by EX05 Ar^+ gun with beam energy of 2 keV. Fitting of the XPS spectra was performed using a Gaussian–Lorentzian peak shape after performing Shirley background correction. The electrical measurements were performed under ambient conditions using the Agilent (B1500A) semiconductor parameter analyzer.

Computation Methodology: The density functional theory (DFT) results were obtained from first-principles plane wave calculation,[50,51] which had been demonstrated to yield rather accurate results for carbon-based materials.[52] The calculation was performed using the spin-polarized local-density approximation (LDA)[53] and projector augmented wave

(PAW)[54] potentials. The kinetic energy cutoff for the plane-wave basis set was taken as 500 eV and a set of 25 × 25 × 1 *K*-point samplings was used for Brillouin zone integration. The convergence criterion for ionic relaxation was 10^{-5} eV between two consecutive steps. By using the conjugate gradient method, all atomic positions and unit cells were optimized until the atomic force was less than 0.02 eV $Å^{-1}$. A vacuum spacing of at least 15 Å was placed between adjacent layers to eliminate the layer–layer interactions. In the calculation of NEB, the periodic hexagonal supercells with 4 × 4 graphene unit cells were utilized. The spring constants between two images were set to be –5 eV $Å^{-2}$ and the Brillouin zone was the 3 × 3 × 1 grid.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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